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An Improvised Version of Reversible Fault Tolerant Carry Skip Adder/Subtractor using Pipeline Technology

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Abstract :- In the recent years, Reversible Logic has drawn attention of researchers due to its less heat dissipating characteristics. It has a wide range of applications in diverse fields such as ultra low power VLSI circuits, nano computing, quantum computing and optical computing. It has a one to one correspondence between its input and output components. Pipelining is also a well known technology for improving the performance of digital systems. We have designed and implemented a new carry skip adder /subtractor using pipelining and parity preserving reversible logic gates. It can be used as a carry skip adder or a carry skip subtractor according to the control logic input. The proposed circuit in this paper is far better than its previous versions in terms of delay, gate count, quantum cost and hardware complexity. The proposed design is designed and implemented using verilog HDL in XILINX 9.2 version. Experimental results demonstrate that the proposed circuit is 68% faster and 65% less complex than its previous versions.

Index Terms :- Reversible logic, Fault Tolerant, Pipelined, Feynman Gate, Fredkin Gate, Modified Islam Gate, Carry skip adder /subtractor.

1. INTRODUCTION

V.N. Landauer [2] and C.H. Bennett [3] , the two major researchers in reversible logic, have shown that every bit of information lost will generate kTlog2 joules of energy, whereas the energy dissipation would not occur, if desigining is done with the help of reversible logic gates. Where k (Boltzmann's constant) = 1.38×10-23 J and T is absolute temperature at which computation process is being performed. Though the energy dissipation for one bit loss is a small value but this value can cause overheating in the circuit which will gradually decrease the life span of the device. And it has been already proved that reversible circuits are the most important solutions of heat dissipation in circuit design.

The Von Neumann Landauer (VNL) [2] principle, a theorem of modern physics, states that ordinary irreversible logic operation which destructively overwrites previous outputs incur a fundamental minimum energy cost. This fact threatens to end improvements in practical computer performance within the next few decades. However, computers based mainly on reversible logic operations can reuse a fraction of the signal energy that theoretically can approach a approximately 100% as the quality of the hardware is improved, at a given level of power dissipation

Fault tolerance is a property which enables a system to continue operating properly even if there is failure in some of its components. If the system is designed by using fault tolerant components, then the correction and detection of faults is possible. Parity preserving gates are used to detect such errors. Many error correction techniques are available. Parity preserving is one of the widely used error detection mechanisms in digital logic and data communication Systems. In parity preserving logic gates, the parity of the inputs must match that of the outputs.

One more factor which is more important than the number of gates used, is the number of garbage outputs. Since reversible design methods use reversible gates, where the number of inputs is equal to the number of outputs, the total number of outputs of such a network will be equal to the number of inputs. Garbage is unavoidable in some cases such as- single output function of n variables will require at least n-1 garbage outputs, because reversibility necessitates an equal number of outputs and inputs.

Reversible Logic Function is a Boolean Function f(x1, x2, x3,….xN) is said to be reversible if it satisfies the following criteria:

(1)The number of inputs should be equal to the number of the number of outputs.

(2)Every output vector should have an unique pre-image.

Reversible Logic Gate is an N-input N-output logic device which provides one to one correspondence between the input and the output. It helps us to uniquely recover the inputs from the outputs. Garbage refers to the number of outputs which are not used in the synthesis of a given function. Quantum Cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is computed knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. Constant Input is the number of inputs that should maintained constant at either 0 or 1 in order to synthesize the given logical function.

Pipelining is a very popular technique for improving the performance of digital systems. It exploits the combinational logic in order to improve throughput. In this technique, we split the combinational logic into two or more than two separate blocks. And blocks are connected with a flipflop. Each block has about less delay than the original block. Since each block has its own registers, every block can operate independently, working on two values at the same time. Thus the cycle time of the machine is reduced because the maximum delay is reduced.

This paper presents a fault tolerant reversible carry skip adder/subtractor using pipelining technology. The reversible logic gates used in this circuit are Feynman gate, Fredkin Gate and Modified Islam Gate. Firstly, a full adder/subtractor is designed using these reversible logic gates. And then a parallel adder/subtractor and a carry skip adder/subtractor is designed with the help of the full adder/subtractor. All these circuits are implemented with the help of pipelining technology

2.PARITY PRESERVING REVERSIBLE LOGIC GATES

A reversible gate is parity preserving gate whose input parity matches the output parity. These are the basic building blocks fault tolerant reversible circuits. Following are some of the basic parity preserving logic gates [4].

2.1 Feynman Double Gate (F2G)

It is a 3*3 gate with input vector I(A,B,C) and output vector O(P=A, Q=A$\oplus$B, R=A$\oplus$C). The quantum cost of this gate is two [6].

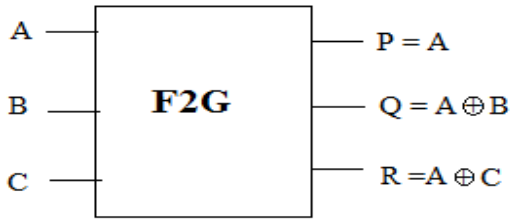

Fig.1 Feynman Double Gate

2.2 Fredkin Gate (FRG)

It is a 3*3 gate with input vector I(A,B,C) and output vector O(P=A, Q=A'B XOR AC, R=A'C XOR AB). The quantum cost of this gate is five[5].

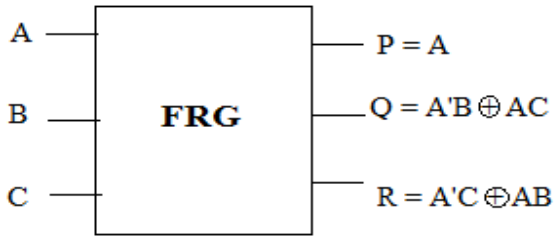

Fig.2 Fredkin Gate

2.3 Modified Islam Gate (MIG)

It is a 4*4 gate with input vector I(A,B,C,D) and output vector O(P=A, Q= A XOR B, R=AB XOR C, S= AB' XOR D). The quantum cost of this gate is seven[7].

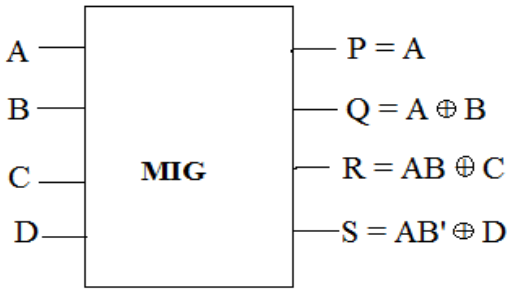

Fig.3 Modified Islam Gate

3. CONVENTIONAL WORK

3.1. Fault Tolerant Full Adder/Subtractor

The following figure shows the previous version reversible fault tolerant full adder/subtractor. It was designed using two Feynman Double gates, two Fredkin gates and two Modified Islam gates[1].

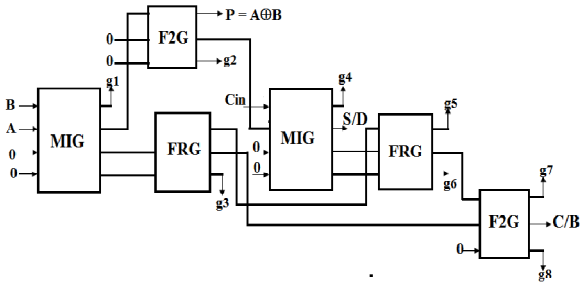

Fig.4 Previous Full Adder/Subtractor

3.1. Fault Tolerant Parallel Adder/Subtractor

The basic building block of parallel adder/subtractor is full adder/subtractor. The given figure shows the previous 4-bit Fault Tolerant Parallel adder/subtractor. It was designed using 4 fault tolerant Full Adder/Subtractor with propagate (p_FT). This design worked as a single unit which includes both parallel adder and subtractor. The control line ctrl was used to select adder or subtractor according the control logic input i.e. when ctrl is 0 it acted as a parallel adder and when ctrl was 1 it acted as parallel subtractor [8].

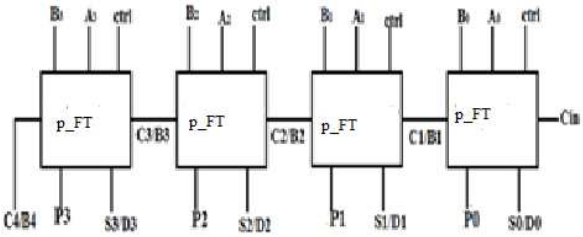

Fig.5 Previous Fault Tolerant 4-Bit Parallel Adder/Subtractor

3.3. Fault Tolerant Carry Skip Adder/Subtractor

In the carry skip adder, delay was reduced due to the carry computation. In the full adder/subtractor operation, if either input was a logical one, the cell would propagate the carry/borrow input to its carry/borrow output. Hence, the nth full adder/subtract or carry/borrow input (C/B)n, would propagate to its carry/borrow output, (C/B)n+1, when Pn = A XOR B. In addition, the multiple full adders/subtractors, making a block can generate a "block" propagate signal P to detour the incoming carry/borrow around to the block's carry/borrow output signal. The given figure shows the previous four bit fault tolerant carry skip adder/subtractor block. It was quickly determined by each block, that whether the block's carry/borrow input was propagated to its carry output. If the block propagate P was one, the block carry/borrow input Cin was propagated as the block carry/borrow output Cout [9].

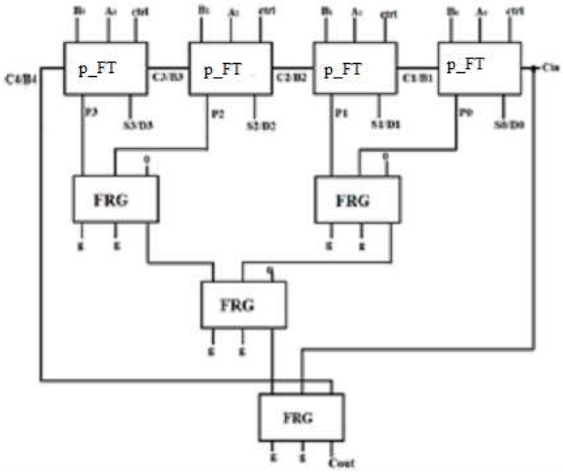

Fig.7 Proposed Fault Tolerant Full Adder/Subtractor with propagate (p_FT)

4.PROPOSED WORK

4.1. Proposed Fault Tolerant Full Adder/Subtractor with propagate (p_FT)

The fault tolerant full adder/subtractor with propagate(p_FT) is shown in the Fig.7 It is designed using Two Modified Islam Gate (MIG), One Fredkin Gate (FRG) and One Feynman Double Gate (F2G).

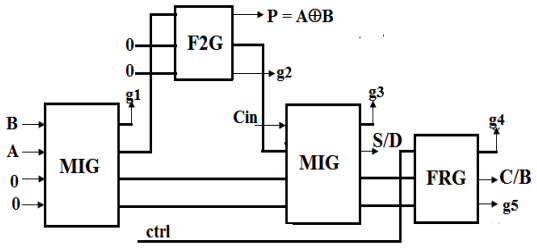

Fig.7 Proposed Fault Tolerant Full Adder/Subtractor with propagate (p_FT)

4.2. Pipelined Fault Tolerant 4-bit Parallel Adder/Subtractor

Full adder/subtractor is the Basic building block of a parallel adder/subtractor. The given figure shows a 4-bit Fault Tolerant Parallel adder/subtractor which is designed using four fault tolerant full adder/subtractor. Also, a flipflop is added between the second and third block as per the pipelining process.

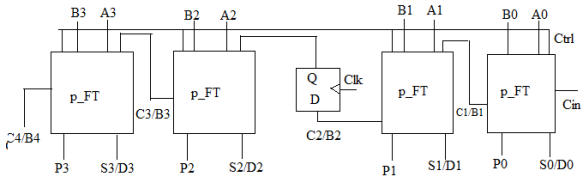

Fig.8 Pipelined Fault Tolerant 4-bit Parallel Adder/Subtractor

4.3 Pipelined Fault Tolerant 4-bit Carry Skip Adder/Subtractor

The proposed Fault Tolerant Carry Skip Adder/Subtractor is the same as the previous version. Only the full adder/subtractor used in the design is that of the proposed version and a flipflop is used between the second and third block. This makes the carry skip adder/subtractor less hardware complex and faster than its previous version.

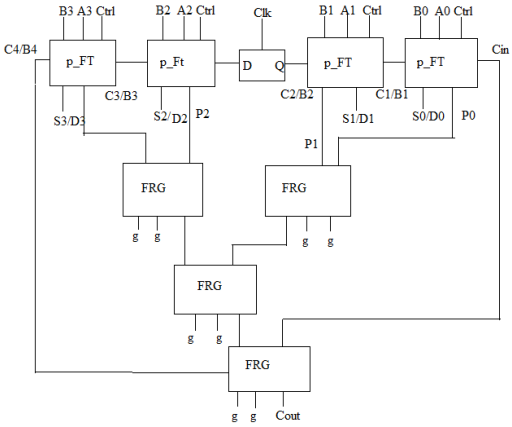

Fig.8 Pipelined Fault Tolerant Carry Skip Adder/Subtractor

5. RESULTS AND COMPARISON

Verilog HDL in Xilinx 9.2 simulator has been taken in use to implement this design. Fig.9, Fig.10 and Fig.11 shows comparison of proposed design of full adder/subtractor, parallel adder/subtractor and carry skip adder/subtractor in terms of gate count and delay respectively.

	Delay	Gate Count	Constant Input	Garbage Output
Previous Full Adder/Subtractor	3.433	6	7	8
Proposed Full Adder/Subtractor	3.433	4	4	5

Table 1. Comparison between Gate Count and Delay of Previous and Proposed Full Adder/Subtractor

	Delay	Gate Count	Constant Input	Garbage Output
Previous Parallel Adder/Subtractor	11.323	20	28	32
Proposed Parallel Adder/Subtractor	3.64	16	16	20

Table 2. Comparison between Gate Count and Delay of Previous and Proposed Parallel Adder/Subtractor

	Delay	Gate Count	Constant Input	Garbage Output
Previous Carry Skip Adder / Subtractor	12.547	28	31	40
Proposed Carry Skip Adder /Subtractor	4.451	20	19	28

Table 3.Comparison between Gate Count and Delay of Previous and Proposed Carry Skip Adder/Subtractor

The Fig. 12 shows simulation results of proposed fault tolerant full adder and full subtractor with propagate, Fig. 13 shows simulation results of pipelined fault tolerant 4-bit parallel adder and parallel subtractor and Fig.14 shows simulation results of pipelined fault tolerant 4-bit carry skip adder and carry skip subtractor.

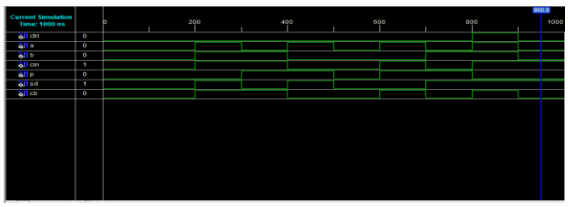

Fig.9 Simulation result of Fault Tolerant Full Adder/Subtractor without pipeline.

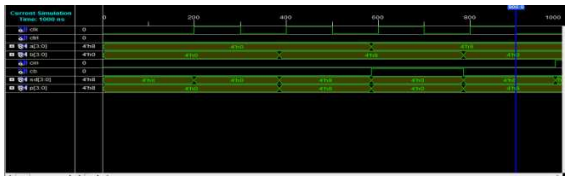

Fig. 10 Simulation result of Fault Tolerant Parallel Adder/Subtractor with Pipelining

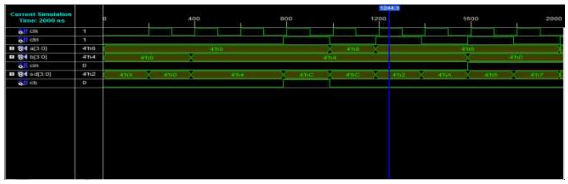

Fig. 11 Simulation result of Fault Tolerant 4-bit Carry Skip Adder/Subtractor

6. CONCLUSION AND FUTURE SCOPE

A less hardware complex and faster carry skip adder/subtractor with the help of pipelining technology has been achieved. The proposed carry skip adder/subtractor have delay lower in comparison to the previous carry skip adder/subtractor. So there are good reasons to believe that a less hardware complex architecture of carry skip adder/subtractor can be easily achieved. In future, one can use this pipeline technology in many other devices such as multipliers, encoders and decoders as this technology is gaining attention among researchers and scholars. This technology reduces the maximum delay which in the end makes the device efficient and fast.

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